UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/525,139	02/16/2005	Emmanuel Ardichvili	FR02 0087	1770

25235 7590 07/07/2010

HOGAN LOVELLS US LLP
ONE TABOR CENTER, SUITE 1500
1200 SEVENTEENTH ST
DENVER, CO 80202

EXAMINER	
FOTAKIS, ARISTOCRATIS	
ART UNIT	PAPER NUMBER
2611	

NOTIFICATION DATE	DELIVERY MODE
07/07/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patent.colorado@hoganlovells.com

Office Action Summary	Application No.	Applicant(s)	
	10/525,139	ARDICHVILI ET AL.	
	Examiner	Art Unit	
	ARISTOCRATIS FOTAKIS	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04/09/2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Reopening of Prosecution After Appeal Brief or Reply Brief

In view of the appeal brief filed on April 09, 2010, PROSECUTION IS HEREBY REOPENED. A new grounds of rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below:

/Shuwang Liu/

Supervisory Patent Examiner, Art Unit 2611

Response to Arguments

Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection. The amendments filed on January 12, 2010 have been entered. Examiner has reopened prosecution in order to clarify his position by introducing the new reference of Hackett as discussed below in the rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1 – 2, 4 – 5, 7, 10 and 12 – 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Medlock et al (US 2002/0037027) in view of Hackett (US 2003/0123528) and further in view of Applicants Admitted Prior Art (AAPA).

Re claims 1, 12 and 13, Medlock teaches of a receiver for receiving an input signal comprising a series of samples (Fig.7), said receiver comprising one delay line (*memory segments of a circular buffer*, Fig.7 or 10, Paragraphs 0025, 0056 and 0063), characterized in that the delay line is configured to delay said input signal by a series of delays (*a series of memory segments 1002a-1002h*, Fig.10) and is divided into a series of delay sub-lines (1004a-h, Fig.10) each sub-line being used to write (FIFO cache, Fig.10) only a single sample (IQ data pair, Paragraph 0063) from the series of samples of said input signal (Paragraphs 0056, 0064 - 0065), each of the delay sub-lines including a separate memory area to receive the single sample from the series of

samples (*memory segments 1002a-1002h*, Fig.10), and further comprising control (Paragraph 0025) means configured to generate, after a last sample of the series of samples is received (*the signal comprising the number of samples (from the first sample to the last sample) are received by the RAKE receiver*), read and write addresses (READ, WRITE Fig.9) of the samples in the delay sub-lines from the series of samples of the input signal (Figs.9 and 10), so that a read address is equal to a difference between the write address of the single sample in a delay sub-line of the input signal (*there is an offset or difference between the READ and WRITE since Reading and Writing is performed in different blocks and not in the same block*), and wherein the delay sub-lines are directly joined to a plurality of multiplexers (plurality of 1012 and 1014a-c) for providing early, in-time, and late outputs (#602, Fig.10), and thereafter to a plurality of demodulators for parallel (*simultaneously*, Paragraphs 0060 and 0065) recombination (RAKE fingers, Fig.10 and Paragraphs 0064 - 0065). Medlock teaches of a delay expressed as a number of sampling periods from the series of delays ("*The blocks in Read mode allow multiple rake fingers with different offsets to read out data sequentially*", Paragraph 0061). However, does not specifically describe or disclose that a read address is equal to a difference between the write address of the single sample in a delay sub-line of the input signal and a delay expressed as a number of sampling periods from the series of delays. Medlock teaches of providing early, in-time, and late outputs to a plurality of demodulators but does not explicitly teach of providing the early, in-time, and late outputs to the plurality of demodulators for parallel recombination in a coherent manner to find common information according to the delay.

Hackett discloses a circular buffer (#60, Fig.5), in the form of a shared memory, and has a memory read pointer (#68, Fig.5) for each rake finger to provide an offset from the location at which the memory write pointer (#60a, Fig.5) writes the data, with the offset being associated with each rake finger receiving a multipath component (Paragraphs 0012 and 0023 - 0025). Therefore, Hacket teaches of a read address (#68) equal to a difference (fine offset) between the write address (#60a) of the single sample in a delay sub-line of the input signal and a delay (chip offset) expressed as a number of sampling periods from the series of delays.

Applicants Admitted Prior Art (AAPA) discloses of a receiver is able to identify and separate the various samples of the copies of the received signal that correspond to the multiple paths so as to recombine them in a coherent manner to find back the common information or the initial input signal (Paragraph 0004).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have the read address equal to a difference between the write address and a delay so as to perform alignment of the multipaths on the shared memory and reduce the number of code generators for the rake receiver. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have the early, in-time, and late outputs, recombined to a plurality of demodulators in a coherent manner so as to recover the initial input signal to its original form according to the delay.

Re claim 2, Medlock teaches of the delay line comprising a single series of delay sub-lines (Fig.9).

Re claim 3, Medlock teaches of the delay line comprising various series of delay sub-lines (Fig.10).

Re claim 4, Medlock teaches of a delay sub-line is accessible with a frequency twice as fast as the samples of an input signal received by the receiver (Paragraphs 0022 - 0024).

Re claim 5, Medlock teaches of wherein one memory area is associated to one delay sub-line (one delay (memory segment) for every bussing element (delay sub-line), Fig.10).

Re claim 6, Medlock teaches of the samples of a series of samples are accessible in parallel in the write mode or read mode in the delay sub-lines (Fig.10, parallel sub-lines 1004a – 1004h). Hackett also teaches of the samples of a series of samples are accessible in parallel in the write mode or read mode in the delay sub-lines (Fig.5 and Paragraph 0022).

Re claim 7, Medlock teaches of the read addresses of the samples of a series of samples are situated at addresses immediately adjacent to one another (Fig.9).

Re claim 8, Medlock teaches of two series of samples are read in parallel (Fig.9, Paragraphs 0061 - 0063).

Re claim 9, Medlock teaches of wherein the delay line comprises selection means of a series of delay sub-lines to which belongs one of the two series of samples read as a function of the delay (#1012, Fig.10).

Re claim 10, Medlock teaches of the delay line comprises a position factor indicating the position of a reference sample from a series of samples of an input signal in the series of delay sub-lines to which it belongs (*Reading and Writing samples to specific memory locations or blocks*, Fig.9).

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Medlock and Applicants Admitted Prior Art (AAPA) in view of Kim et al (US 6,788,731).

Medlock and AAPA teach all the limitations of claim8 as well as Medlock teaches of the memory areas for a series of samples read (Paragraphs 0063 – 0064, Fig.10) which correspond to a first and second series of delay sub-lines (Fig.10). However, Medlock and AAPA do not specifically teach of that the memory areas are regrouped into a first and a second group, the first group regrouping a current series of

current areas and a next series of areas which can each correspond to the first series of delay sub-lines and the second group regrouping the current series of areas and the next series of areas which can each correspond to the second series of the delay sub-lines, so that the memory areas for a series of samples read are identical for each equal position factor value.

Kim teaches of that the memory areas are regrouped into a first and a second group (BANK 0 and BANK 1, Figs.6 - 7), the first group (BANK 0) regrouping a current series of current areas (0 – 7, Fig.7) and a next series of areas (16 – 23, Fig.7) and the second group (BANK 1) regrouping the current series of areas (8 – 15, Fig.7) and the next series of areas (24 – 31, Fig.7), so that the memory areas for a series of samples read are identical for each equal position factor value (#306, Fig.9).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have regrouped into two groups the samples from the delay lines in the FIFO cache of Medlock so as to increase and reduce processing time of the system.

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Medlock in view of Hackett in view of AAPA and further in view of Kim et al (US 6,788,731).

Medlock, AAPA and Kim teach of a receiver for receiving an input signal comprising a series of samples, said receiver comprising one delay line, characterized

in that the delay line is configured to delay said input signal by a series of delays and is divided into a series of delay sub-lines each being used to write one from the series of samples of said input signal, each of the delay sub-lines including a memory area to receive at least one sample from the series of samples, and further comprises control means configured to generate read addresses of the samples in the delay sub-lines from the series of samples of the input signal, so that a read address is equal to a difference between a write address of a sample in a delay sub-line of the input signal and a delay expressed as a number of sampling periods from the series of delays, wherein the delay line comprises various series of delay sub-lines, two series of samples are read in parallel, and the memory areas are regrouped into a first and a second group, the first group regrouping a current series of current areas and a next series of areas which can each correspond to the first series of delay sub-lines and the second group regrouping the current series of areas and the next series of areas which can each correspond to the second series of the delay sub-lines, so that the memory areas for a series of samples read are identical for each equal position factor value (see claims 1 and 11).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ARISTOCRATIS FOTAKIS whose telephone number is (571)270-1206. The examiner can normally be reached on Monday - Friday 6:30 - 4.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh M. Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Aristocratis Fotakis/

Examiner, Art Unit 2611
/Shuwang Liu/
Supervisory Patent Examiner, Art Unit 2611